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10/725,888	02/04/2004	William J. Borland	EL0497USNA	3392

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EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/725,888	Applicant(s) BORLAND ET AL.	
	Examiner Hoa C. Nguyen	Art Unit 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *6-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5 pgs*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of claims 1-5, 11-16 and 21-25 in the reply filed on 3/20/06 is acknowledged.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct species:

Species I: Figures 1-4 drawn a structure of a stacked capacitors connecting in parallel, wherein the capacitors' electrodes are formed in parallel on top of each other.

Specie II: Figures 5A-5I drawn to a structure of a plurality of capacitors formed in a multilayer circuit board, wherein each capacitor has three electrodes, at least two of the electrodes have termination sections formed thereon, and dielectric layers formed in between the electrodes are not contiguous.

Specie III: Figures 6A-6D drawn to a structure of a plurality of capacitors formed in a multilayer circuit board, wherein each capacitor has five electrodes.

Specie IV: Figures 7A-7B drawn to a structure of a capacitor formed in a multilayer circuit board, wherein the capacitor has at least three electrodes and at least two electrodes formed on both side of a foil electrode.

Specie V: Figures 8A-10B drawn to a structure of a capacitor formed in a multilayer circuit board, wherein the capacitor has two electrodes and a trench formed in between one of the electrode.

The species are independent or distinct because each specie drawn to a different structure.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claim 1 is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

3. During a telephone conversation with applicants' attorney, Mrs. Barbara C. Siegell, on 4/5/06 a provisional election was made with traverse to prosecute the invention of specie I, claims 1-5 (figures 1-4). Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-16 and 21-25 are further withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one

or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

~~Specification~~ CLAIM OBJECTION

4. Claim 2 is objected to because of the following informalities: In claim 2, first line: "... claim 1, comprising:" must be changes to "... claim 1, **further** comprising:". Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakano et al. (US 6785121).

Regarding claim 1, as shown in figure 1, Nakano et al. disclose a printed wiring board, comprising:

(a) A first innerlayer panel (any number of layers shown in the figure can be arbitrary group into a panel - all dielectric layer and electrodes are denoted by reference characters 2 and 3 respectively), the first innerlayer panel (considering the bottom layers as a first innerlayer panel) comprising:

(b) a first electrode 3 (considering the first electrode 3 from the bottom of the stack shown in the figure), see column 3, lines 28-48;

(c) a dielectric 2 (considering the dielectric disposed on top of the first electrode) disposed over the first electrode 3;

(d) a second electrode 3 (considering the electrode on top of the first one spaced apart by a dielectric layer) disposed over the dielectric,

(c) the first electrode, the dielectric and the second electrode form a first capacitor (noticed: a pair of conductive layers sandwiches a thin layer of dielectric material inherently forms a capacitor);

(e) a second innerlayer panel (any number of layers formed on top of the above capacitor can be arbitrary group into a panel), the second innerlayer panel comprising:

(f) A first electrode 3;

(g) a dielectric disposed over the first electrode;

(h) a second electrode disposed over the dielectric,

(i) the first electrode, the dielectric and the second electrode form a second capacitor,

(j) the second innerlayer panel is stacked with the first innerlayer panel, the respective first electrodes are electrically coupled through a conductive via (no number - to form one of external electrodes 4), and the respective second electrodes are electrically coupled through a conductive via (no number - to form another external electrode 4), thereby connecting the first and second capacitors in parallel.

It is noticed that Nakano et al. disclose a plurality of dielectric and electrode layers formed parallel on top of each other. Any group of layering structure with dielectric layers sandwiched between at least two conductive layers conventionally formed a capacitor. The capacitors are stacked on each other and connected in parallel forming a larger storage capacitor. In one of examples, Nakano et al. disclose a stacked capacitor with electrodes formed on a stack of 100 layers of dielectric material, see column 8, lines 63-66.

Regarding claim 2, as shown in figure 1, Nakano et al. disclose every limitation as shown in claim 1 above inherently including a third capacitor, fourth capacitor, fifth capacitor, ..ect.., stacked on top of each other and electrically connected in parallel.

Regarding claim 3, as shown in figure 1, Nakano et al. disclose every limitation as shown in claim 1 above including a third electrode spaced from the second electrode by the dielectric and electrically coupled to the first electrode, wherein the dielectric is a two-layer dielectric.

Regarding claim 4, as shown in figure 1, Nakano et al. disclose every limitation as shown in claims 1 and 3 above including a fourth electrode spaced from the third electrode by the dielectric and electrically coupled to the second electrode, wherein the dielectric is a three-layer dielectric.

Regarding claim 5, as clearly shown in figure 1, Nakano et al. disclose the respective first and second electrodes are electrically coupled by a first and second conductive via (no number, conductive vias for external electrodes 4 for external connections).

Citation of Relevant Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Zavrel et al. (US 6218729) disclose an apparatus and method for an integrated circuit having high Q reactive components.

Kola et al. (US 6005197) disclose an embedded thin film passive components.

Chakravorty (US 6970362) discloses an electronic assemblies and systems comprising interposer with embedded capacitors.

Chakravorty (US 6611419) discloses an electronic assembly comprising substrate with embedded capacitors.

Branchevsky (US 6252761) discloses an embedded multi-layer ceramic capacitor in a low-temperature con-fired ceramic (LTCC) substrate.

Li et al. (US 6636416) disclose an electronic assembly with laterally connected capacitors and manufacturing method.

Naito et al. (US 6344961) disclose a Multi-layer capacitator, wiring substrate, decoupling circuit, and high-frequency circuit.

Stevenson et al. (US 6888715) disclose an EMI feedthrough filter terminal assembly utilizing hermetic seal for electrical attachment between lead wires and capacitor.

Li et al. (US 6519134 Universal capacitor terminal design.

Sogabe et al. (US 5870273) disclose a Multi-functional multilayer device and method for making.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Hoa C. Nguyen
4/6/06

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